	Type	L #	Hits	Search Text	DBs
1	BRS	L1	14035	(scatter$3 gather$3) near10 (bit byte element item)	USPAT; US-PGPUB
2	BRS	L3	5584	(scatter$3 gather$3) near10 (bit byte element item)	EPO; JPO; DERWENT
3	BRS	L2	144	1 near20 mask$3	USPAT; US-PGPUB
4	BRS	L4	44	3 near20 mask$3	EPO; JPO; DERWENT; IBM_TDB
5	BRS	L6	2739	(scatter$3 gather$3) near20 mask$3	USPAT; US-PGPUB
6	BRS	L10	47646	(reorder$3 order$3 rearrang$3 arang$3) near10 (bit byte element item)	EPO; JPO; DERWENT; IBM_TDB
7	BRS	L11	1026	(scatter$3 gather$3) near20 mask$3	EPO; JPO; DERWENT; IBM_TDB
8	BRS	L12	4	10 and 11	EPO; JPO; DERWENT; IBM_TDB
9	BRS	L9	103	(reorder$3 order$3 rearrang$3 arang$3 scatter$3 gather$3).ab,ti. and 7	USPAT; US-PGPUB
10	BRS	L13	351267	(reorder$3 order$3 rearrang$3 arrang$3) near10 (bit byte element item)	USPAT; US-PGPUB
11	BRS	L14	170489	(reorder$3 order$3 rearrang$3 arrang$3) near10 (bit byte element item)	EPO; JPO; DERWENT; IBM_TDB
12	BRS	L16	593	6 and 13	USPAT; US-PGPUB
13	BRS	L18	15	11 and 14	EPO; JPO; DERWENT; IBM_TDB
14	BRS	L17	171	(reorder$3 order$3 rearrang$3 arrang$3 scatter$3 gather$3).ab,ti. and 16	USPAT; US-PGPUB
15	BRS	L19	139	17 not 2	USPAT; US-PGPUB
16	BRS	L20	5452	gather$3 near10 (bit byte element item)	USPAT; US-PGPUB
17	BRS	L21	22	20 near50 mask$3	USPAT; US-PGPUB
18	BRS	L22	301	permut$4.ab,ti.	USPAT; US-PGPUB
19	BRS	L23	45	22 and mask$3	USPAT; US-PGPUB
20	BRS	L26	55	permut$4 near99 mask$3 not 23	USPAT; US-PGPUB
21	BRS	L27	2	permut$4 near99 mask$3	EPO; JPO; DERWENT; IBM_TDB

modulation/demodulation method is not limited to the aforementioned ones.

The transmission serial data signal (k) output from the EXOR circuit 212 is serially output as the transmit data through an AND gate 213. At that time, output or non-output of the transmit data is controlled by signals (m) and (l). The signal (l) assumes the "low" level when an error is detected from the result of the comparison made by the comparing/selecting circuit 20 and from the result of the error detecting circuit 7, and thereby interrupts output of the transmit data (details being described later). The signal (m) is at the logical "high" level only during the shift out of the 8-bit shift register 16 which is controlled by the timing generating circuit 3, and thereby allows for the output of the transmit data.

FIG. 3 is the timing chart of this modulation operation. In FIG. 3, the signal (l) is in a state in which no error is occurring. The states of the serial data output, (l), (j), $/\phi_{32}$, (k) and (m) located at the respective points indicated in FIG. 2 are shown in FIG. 3 as the functions along the time dimension (hereinafter /X represents inverted X).

The operation of the demodulating/converting circuit 6 and that of the modulation error detecting circuit 7 will be described below.

In FIG. 2, the receive data is first input to the synchronizing circuit 4. The synchronized receive data (a) is input to a D flip-flop 61 (hereinafter a flip-flop being referred to as a F/F). The multiple frequency dividing circuit 2 is reset and initialized by the frequency-division control circuit 5 synchronized by the synchronizing circuit 4 and thereby starts counting. The D-F/F 61 is triggered by a clock ϕ_{16} obtained by the multiple frequency demodulating circuit 2. Output (e) of the D-F/F 61 is input to both an EXOR circuit 72 and a D-F/F 71. The D-F/F 71 is triggered by the same clock as the D-F/F 61. Output (f) of the D-F/F 61 is input to the other input of the EXOR circuit 72. A signal (b) from the timing circuit 3 is input to the set terminal of the D-F/F 61 and to the reset terminal of the D-F/F 71. The EXOR circuit 72 compares the outputs of the D-F/Fs 61 and 71, and the results of the comparison is input to a JK-F/F 73. The JK-F/F 73 is triggered by a clock ϕ_{32} obtained by the multiple frequency dividing circuit 2, detects an error from the results of the demodulation, and outputs an error signal (h). That is, the EXOR circuit 72 checks whether or not each data bit is a combination of "0" and "1", that is, in the example of the modulating circuit, the EXOR circuit 72 checks whether or not 1 and 0 are respectively represented by "10" and "01". If the answer is negative, the JK-F/F 73 is set to raise the error signal (h).

An inverted output (i) of the D-F/F 61 is input to the shift in terminal of the 8-bit shift register 16. Since the shift clock of the 8-bit shift register 16 is the clock ϕ_{32} obtained by the multiple frequency dividing circuit 2, the inverted output of the D-F/F 61 is latch shifted alternately.

FIG. 4 is a timing chart of the above-described operation. FIG. 4 shows the states of (a), ϕ_{32}, ϕ_{16}, (b), (c), (e), (f), (h) and (i) which are located at the respective points shown in FIG. 2.

The digital modulation/demodulation means for modulating the output data of the serial communication under a predetermined condition to obtain an output signal and for demodulating the input signal under a predetermined condition to obtain an input data, as well as an error detection means for detecting an error in accordance with modulation/demodulation regulations when the input signal is demodulated by the digital modulation/demodulation means, have been described.

Next, parallel data of the 8-bit shift register 16 shown in FIG. 2 and the signal (l) will be described in detail with reference to FIGS. 5 to 8.

When demodulated data (z) is present in 8 bits as a consequence of the shifting of the receive data (i), the 8-bit data is input in a first shift data latch circuit 17 by means of a latch pulse (w) from the timing generating circuit 3. Thereafter, when another 8 bits of the demodulated data (z) are present after the 4 bits have been passed by, the 8-bit data is input to a second shift data latch circuit 18 by means of a latch pulse (v) from the timing generating circuit 3. Finally, when another 8 bits of the demodulated data (z) are present after the 3 bits have been passed by, the 8-bit data is input to a third shift data latch circuit 19 by means of a latch pulse (u) from the timing generating circuit 3. In other words, in this embodiment, space bits, i.e., dummy bits, are inserted in one frame, so that the bits in a predetermined duration can be made effective on the time-series basis. It is to be noted that even the space bits are serially communicated in a modulated state.

The data respectively latched in the shift data latch circuits 17, 18 and 19 are input to the comparing circuit 20 for comparison which is made under a predetermined condition. In this embodiment, comparison is made under the following conditions: the demodulated data (z) is input in the order of "1, 0, ID2, ID1, D7, D6, D5, D4, X, X, X, X, D3, D2, D1, D0, /D0, /D1, /D2, /D3, X, X, X, /D4, /D5, /D6, /D7, /ID2, /ID1, /ID0, ID0, X", as shown in FIG. 7 (Dn represents data, and /Dn represents inverted data. X represents space bit and is practically "0"). Hence, comparison is made under the predetermined condition shown in FIG. 6.

After comparison, the individual outputs of the EXOR circuits are put together by an NAND gate 201 which outputs an output (n). This data comparison signal (n), together with a demodulation error signal (h), is input to an NOR gate 202 designed to output a signal (l). That is, the data comparison signal (n) assumes a high level if comparison error exists even in a single bit, and thereby lowers the signal (l) regardless of the state of the error signal (h) obtained by the checking conducted during demodulation. As a result, the output of the AND gate 213 is interrupted, and no transmit data is output.

FIG. 7 is a timing chart for the shift data latch circuit and the comparison/selection circuit. The timing chart shown in FIG. 7 is that for the reception of normal data. The signal (n) falls after completion of reception of the demodulated data (z). At that time, since the error signal (h) is also at the logical low level because of no error, the signal (l) rises and thus permits output of the AND gate 213. This enables output of the transmit data. At the same time, the signal (l) also opens the AND gate 22. Consequently, a latch pulse (t) from the timing generating circuit 3 is loaded in the data output circuit 10, and the output data is thereby output. In FIG. 7, (w), (v), and (u) respectively represent the latch pulses from the timing generating circuit 3 for giving load pulses the shift data latch circuits 17, 18 and 19. As these latch pulses are given to the shift data latch circuits, the first, second and third latch data are latched for generation of the comparison result signal (n) shown in FIG. 6. The receive data is thus taken in the communication means.

	Document ID	U	Title	Current OR
1	US 20030171908 A1	☐	Simulation and timing control for hardware accelerated simulation	703/16
2	US 20020116602 A1	☐	Partial bitwise permutations	712/223
3	US 20020016581 A1	☐	Absorbent article with improved surface fastening system	604/386
4	US 20010014936 A1	☐	Data processing device, system, and method using a table	711/221
5	US 6687801 B1	☐	Adaptive copy pending off mode	711/162
6	US 6631369 B1	☐	Method and system for incremental web crawling	707/4
7	US 6549959 B1	☐	Detecting modification to computer memory by a DMA device	710/22
8	US 6397379 B1	☐	Recording in a program execution profile references to a memory-mapped active device	717/140
9	US 6330333 B1	☐	Cryptographic system for wireless communications	380/207
10	US 5830064 A	☐	Apparatus and method for distinguishing events which collectively exceed chance expectations and thereby controlling an output	463/22
11	US 5818337 A	☐	Masked passive infrared intrusion detection device and method of operation therefore	340/567
12	US 5727064 A	☐	Cryptographic system for wireless communications	380/270
13	US 5598410 A	☐	Method and apparatus for accelerated packet processing	370/469
14	US 5534893 A	☐	Method and apparatus for using stylus-tablet input in a computer system	345/179
15	US 5517660 A	☐	Read-write buffer for gathering write requests and resolving read conflicts based on a generated byte mask code	711/117
16	US 5471628 A	☐	Multi-function permutation switch for rotating and manipulating an order of bits of an input data byte in either cyclic or non-cyclic mode	712/223
17	US 5463476 A	☐	Image processing system	358/426.02
18	US 5282151 A	☐	Submicron diameter particle detection utilizing high density array	702/26
19	US 5224214 A	☐	BuIffet for gathering write requests and resolving read conflicts by matching read and write requests	710/39
20	US 5170263 A	☐	Image processing system	358/3.29
21	US 5123095 A	☐	Integrated scalar and vector processors with vector addressing by the scalar processor	712/218

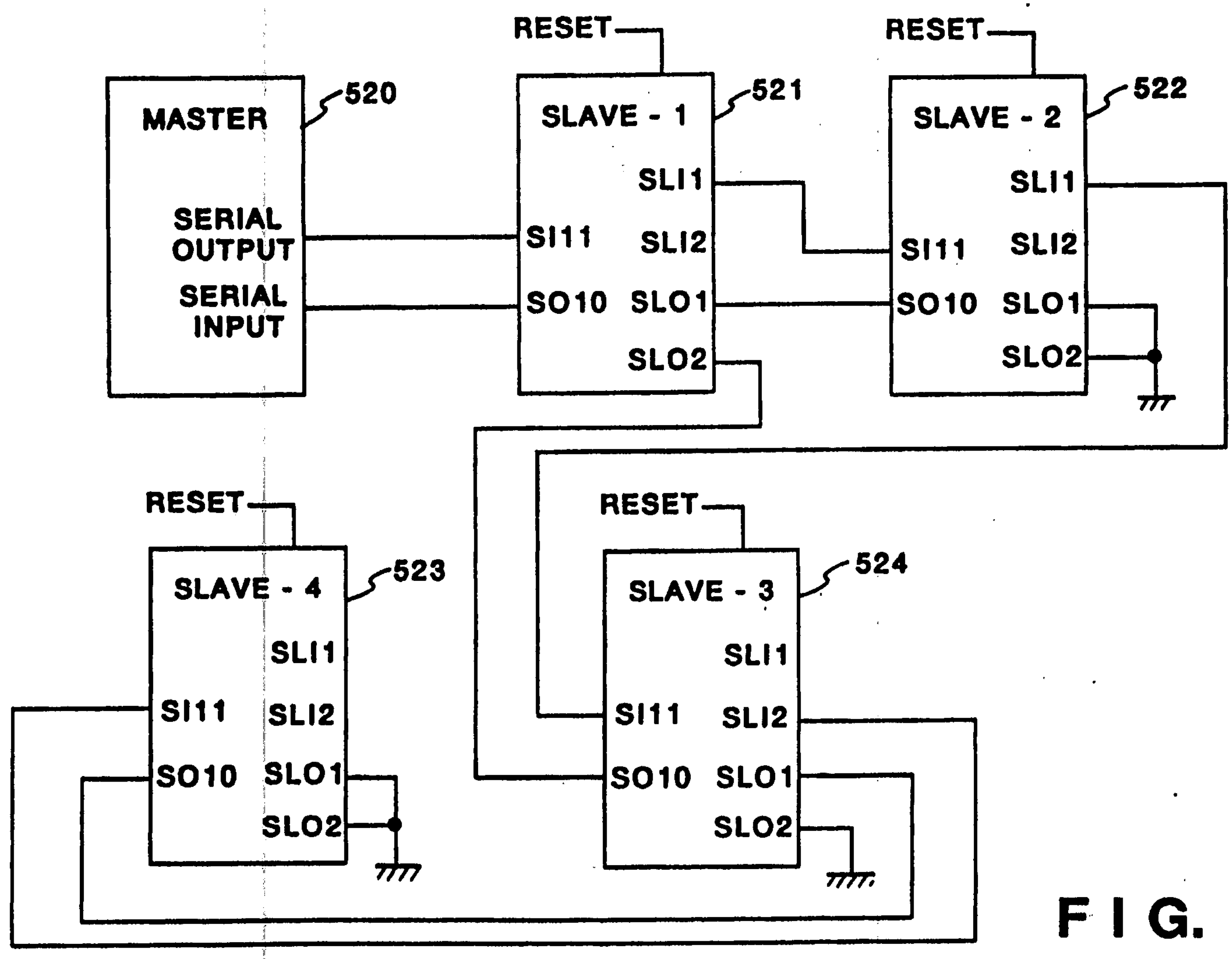
MASTER
SERIAL OUTPUT
SERIAL INPUT
520
RESET
SLAVE - 1
SLI1
SI11
SLI2
SO10
SLO1
SLO2
521
RESET
SLAVE - 2
SLI1
SI11
SLI2
SO10
SLO1
SLO2
522
RESET
SLAVE - 4
SLI1
SI11
SLI2
SO10
SLO1
SLO2
523
RESET
SLAVE - 3
SLI1
SI11
SLI2
SO10
SLO1
SLO2
524

FIG. 43

	Document ID	U	Title	Current OR
22	US 3972598 A	☐	Multifaceted mirror structure for infrared radiation detector	359/853

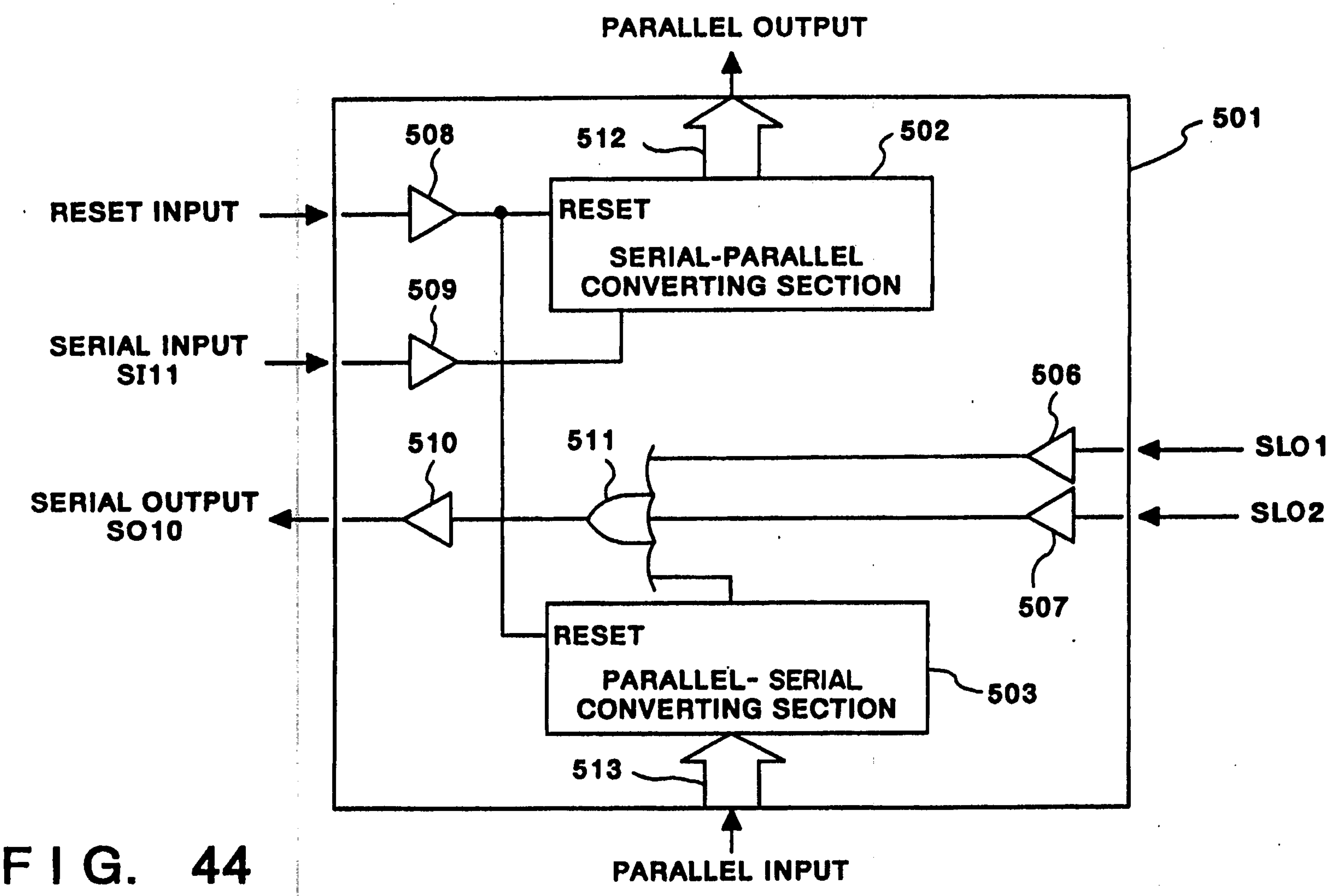
PARALLEL OUTPUT
501
508
512
502
RESET INPUT
RESET
SERIAL-PARALLEL CONVERTING SECTION
509
SERIAL INPUT SI11
506
510
511
SLO1
SERIAL OUTPUT SO10
SLO2
507
RESET
PARALLEL- SERIAL CONVERTING SECTION
503
513
PARALLEL INPUT

FIG. 44

	Document ID	U	Title	Current OR
1	US 20040057928 A1	☐	Use of il-6r/il-6 chimera in huntington's disease	424/85.2
2	US 20040025032 A1	☐	Method and system for resistance to statiscal power analysis	713/189
3	US 20040008841 A1	☐	Method and apparatus for data permutation/division and recording medium with data permutation/division program recorded thereon	380/42
4	US 20030195915 A1	☐	Method and apparatus for data permutation/division and recording medium with data permutation/division program recorded thereon	708/650
5	US 20030172254 A1	☐	Instructions for manipulating vectored data	712/224
6	US 20020184480 A1	☐	Vectorized table lookup	712/300
7	US 20020159501 A1	☐	Data transmission and reception within a spread-spectrum communication system	375/130
8	US 20020126124 A1	☐	Planar byte memory organization with linear access	345/533
9	US 20020118827 A1	☐	Block cipher method	380/37
10	US 20020108030 A1	☐	Method and system for performing permutations using permutation instructions based on modified omega and flip stages	712/300
11	US 20020078011 A1	☐	Method and system for performing permutations with bit permutation instructions	707/1
12	US 20020031220 A1	☐	Method and system for performing permutations using permutation instructions based on butterfly networks	380/37
13	US 20020012386 A1	☐	Method and apparatus for the construction and transmission of binary quasi orthogonal vectors	375/146
14	US 20010038693 A1	☐	Block cipher method	380/37
15	US 20010031010 A1	☐	Method and apparatus for the reflection and transmission of quasi orthogonal vectors	375/242
16	US 6704904 B1	☐	Method and apparatus for permuting code sequences and initial context of code sequences for improved electrical verification	714/819
17	US 6640327 B1	☐	Fast BCH error detection and correction using generator polynomial permutation	714/785
18	US 6611566 B2	☐	Reflection and transmission of quasi orthogonal vectors	375/295

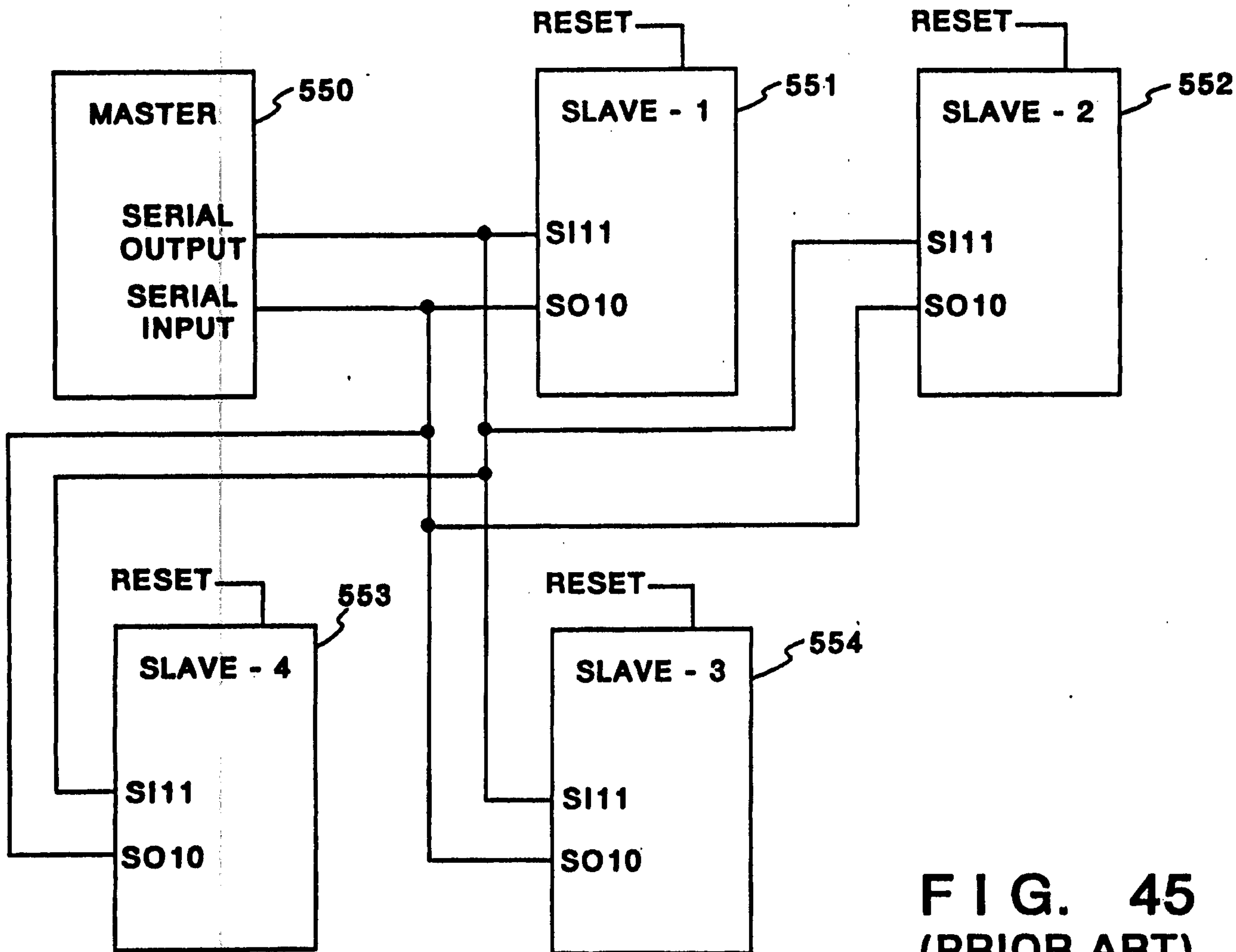

FIG. 45
(PRIOR ART)

	Document ID	U	Title	Current OR
19	US 6578150 B2	☐	Block cipher method	713/200
20	US 6578061 B1	☐	Method and apparatus for data permutation/division and recording medium with data permutation/division program recorded thereon	708/520
21	US 6446198 B1	☐	Vectorized table lookup	712/300
22	US 6314125 B1	☐	Method and apparatus for the construction and transmission of binary quasi orthogonal vectors	375/130
23	US 6240143 B1	☐	Method and apparatus for the reflection and transmission of quasi orthogonal vectors	375/295
24	US 6233337 B1	☐	Methods and apparatus for enhanced security expansion of a secret key into a lookup table for improved security for wireless telephone messages	380/28
25	US 6199162 B1	☐	Block cipher method	713/168
26	US 6182216 B1	☐	Block cipher method	713/168
27	US 6157611 A	☐	Method and apparatus for transmission and construction of quasi orthogonal vectors	370/208
28	US 6125182 A	☐	Cryptographic engine using logic and base conversions	380/28
29	US 6091760 A	☐	Non-recursively generated orthogonal PN codes for variable rate CDMA	375/140
30	US 5956351 A	☐	Dual error correction code	714/757
31	US 5843279 A	☐	Cellulosic fibrous structures having at least three regions distinguished by intensive properties	162/109
32	US 5834181 A	☐	High throughput screening method for sequences or genetic alterations in nucleic acids	435/5
33	US 5804281 A	☐	Cellulosic fibrous structures having at least three regions distinguished by intensive properties	428/137
34	US 5619576 A	☐	Variable-key cryptography system	380/44
35	US 5425103 A	☐	Variable-key cryptography system	380/44
36	US 5335280 A	☐	Random sum cipher system and method	380/42
37	US 5277761 A	☐	Cellulosic fibrous structures having at least three regions distinguished by intensive properties	162/109
38	US 5272671 A	☐	Semiconductor memory device with redundancy structure and process of repairing same	365/200
39	US 4972475 A	☐	Authenticating pseudo-random code and apparatus	380/54
40	US 4882683 A	☐	Cellular addressing permutation bit map raster graphics architecture	345/568
41	US 4771384 A	☐	System and method for fragmentation mapping	382/129

COMMUNICATION SYSTEM FOR DETECTING A COMMUNICATION ERROR IN INFORMATION TRANSMITTED BETWEEN A PLURALITY OF UNITS AND A MAIN CONTROL UNIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a unit control oriented communication device for exchanging information between a group of units scattered inside and outside of a system and a main control section for controlling the group of units, and more particularly, to an optical radio communication device which utilizes light (hereinafter referred to as a wireless optical communication device).

2. Description of the Related Art

Conventionally, a copier, a FAX, or a laser beam printer (hereinafter referred to as an LBP) is composed of a main control portion for controlling the entire system and a group of units scattered inside and outside of the system. The group of units are each composed of an output control section comprising a motor, a fan or an actuator, such as a solenoid, and an input control section comprising switches and sensors. In that case, the input/output control sections are respectively controlled mainly through an I/O port of a CPU. Since these input/output control subjects are scattered within the system, they are connected with each other through a wire harness. These input/output control subjects are connected to the main control portion independently from each other (hereinafter referred to as parallel connection). Alternatively, the main control portion serially transfers data to each unit utilizing serial communication. Each unit conducts "serial-parallel conversion", by which the control subjects are connected to the main control portion independently.

An example of the aforementioned parallel connection will be described. In the case of a system shown in FIGS. 31 and 32 which consists of units **406** and **407**, the unit **406** serves as a control unit, and the unit **407** serves as a controlled unit (on which a mechanism part, such as a solenoid, is mounted). In this case, a CPU **301** is connected through signal lines directly to respective mechanism portions **401**, **402**, **403** and **404** in the controlled unit (FIG. 31) to control them. Although an amplification means or the like, such as a transistor, is disposed between the control unit **406** and the controlled unit in an actual circuit configuration, it is omitted in FIGS. 31 and 32 in order to explain the flow of signals.

In another case, the subjects to be controlled are controlled by the CPU **301** through an I/O expansion device **301a**, as shown in FIG. 32.

In the above-described methods, the number of signal lines (signal line bundles) increases in proportion to the number of subjects to be controlled, and this makes reduction in the overall size of the system difficult.

That is, as the number of functions of the system increases, the number of input/output control subjects increases, thereby increasing the number of control lines for parallel connection. As a result, production cost increases, and assembly efficiency deteriorates. Hence, the general trend is toward an arrangement of scattered output and input signals into a plurality of physical or functional blocks and transmission of signals by the serial communication.

Serial communication commonly conducted between the main control portion and the group of units is asynchronous serial communication, called UART, or clock synchronizing type serial communication.

In the former type of serial communication, a single frame consists of twelve bits, including a starting bit (1 bit), a data bit, and a stop bit (2 bits). The transmission side outputs a signal representing one frame with a predetermined period. The reception side reads data representing one frame at the same period as the transmission side when it confirms the starting bit.

In the latter type of serial communication, a single frame consists of eight bits. The transmission side outputs a signal representing one frame with a clock signal and a data signal separately through corresponding paths. The reception side reads the status of the data signal at a timing at which a clock signal rises or falls and receives data representing one frame.

However, the above-described conventional methods have the following disadvantages.

(1) In the method of decreasing the number of control lines by conducting serial transfer from the main control portion utilizing serial communication such as UART, a malfunction may occur due to the erroneous transfer caused by noise generated in the system, or the control line may generate radiation noises in the form of an electric field as the serial transfer speed increases.

To overcome this disadvantage, radio transmission of data using light has been considered.

In the field of electric appliances, radio transmission of data using light, so-called remote control, has been conducted. However, such a system is of the unidirectional type (in which data is transmitted only from the transmission device to the reception device). Furthermore, the data transmission speed is such that it cannot catch up with the transmission speed of input/output signals in, for example, a copier, FAX or LBP. Furthermore, when optical transfer is conducted at a relatively high speed in two directions, collision of light or erroneous transmission caused by a disturbance may occur. Also, the existence or non-existence of the reception device cannot be determined at the main control portion. Furthermore, adjustment or checking conducted during the assembly is troublesome, and reduces efficiency.

(2) Although there is no problem in the case of transmission of a signal consisting of one bit, when a signal consisting of a plurality of bits is to be transmitted, all the bits do not change at one time, and transmission of an erroneous signal may thus occur unless data latching is not adjusted.

This problem will be explained in detail with reference to FIG. 33.

In the case shown in FIG. 33, communication is made between the units **406** and **407** through a communication line **405**. The communication line **406** may be parallel or serial. This choice is made depending on the transfer speed or the application of the transfer. Although this communication is more advantageous when a plurality of units **407** to be controlled exist, the units **406** and **407** make one-to-one correspondence in this case for the ease of explanation.

A CPU **301** and a transmission means **409** function independently. The CPU **301** sends transmit data to a transmission register **408**. The transmission means **409** transfers the content of the transmission register **408** to the unit **407** at predetermined time intervals. A reception means **302** transfers the received data to the individual mechanism sections **401**, **402**, **403** and **404**.

	Document ID	U	Title	Current OR
42	US 4598170 A	☐	Secure microprocessor	713/190
43	US 4543646 A	☐	Chip topography for MOS Data Encryption Standard circuit	380/29
44	US 4524427 A	☐	Method for making comparisons between reference logical entities and logical entities proceeding from a file	707/6
45	US 4430571 A	☐	Method and apparatus for exposing multi-level registered patterns interchangeably between stations of a multi-station electron-beam array lithography (EBAL) system	250/492.2

In order to control the unit 407, monitoring of an external status is required. Fetching of externally monitored signals to the CPU 301 through the communication line will be described below with reference to FIG. 34.

A signal from sensors (for example, microswitches or photo-interruptors) 410, 411, 412 and 413 is transferred from a transmission means 303 to a reception means 414. A communication line 416 which connects the transmission means 303 and the reception means 414 may be of the parallel or the serial type. The reception means 414 writes receive data in a reception register 415. The reception register 415 is connected to the CPU 301, and the CPU 301 can read the content thereof at a desired time. That is, new data (which represents the state of the mechanism sections 410, 411, 412 and 413, in this case) is kept stored in the reception register 415.

The transmission register 408 and the reception register 415 will be described in more detail.

FIG. 35 explains the operation of the transmission register 408. The transmission register 408 is required for the CPU 301 and the transmission means 409 being operated independently. The number of bits for the register 408 must be made to coincide with the total number of bits in the destination unit.

In order to conduct mapping between the transmission register 408 and the CPU 301 and thereby assign a certain address of the CPU 301 to the register 408, a write signal 438 is created by decoding an address signal on an address bus 434 by means of a decoder 435 and then by performing an AND operation on the decoded address signal and a write signal 433. The transmit data is transferred to the transmission register 408 synchronously with the write signal 438.

The transmission means 409 latches the content of the transmission register 408 synchronously with a latch signal 439 from a control circuit 437. That is, the transmission means 409 takes in data from the transmission register 408 to its latches corresponding to the bits of the data, e.g., the data in a latch 417 is latched to a latch 425, the data in a latch 418 is latched to a latch 426, and so on. Thereafter, the transmission means 409 conducts transmission operation independently.

Next, the reception register 415 will be described in detail with reference to FIG. 36. Once the reception means 414 receives data from the transmission means 303 of the external unit 407, it outputs a write pulse 452 and latches the data in latches 440 to 447 of the reception register 415. The receive data is read by the CPU 301 from the reception register 415 by means of a signal obtained by decoding an address signal 434 output from the CPU 301 for mapping by a decoder 448 and then by performing an AND operation on the decoded signal and a read signal 449.

Unit control is thus performed through the communication lines 405 and 416.

In a case where data is transmitted from the CPU 301 to the unit 407, the timing of the write signal 438 of the CPU 301 may differ from that of the read-out signal 439 of the unit, as shown in FIG. 37. In that case, data 453 output from the CPU 301 may be latched in the transmission register 408 at a time indicated by data 454 in FIG. 37, and that data may be read in the transmission means 409 at a time indicated by data 455 in FIG. 37. Erroneous transmission of the data does not occur when the data is read in the transmission means 409 at a time other than a transition of the data 454, as in the case of the above-described case. The same thing applies to the case in which data is transmitted to the CPU 301. In the case shown in FIG. 36, data 457 from the reception means 414 is latched in the reception register 415 by the write signal 452 at a time indicated by data 456 in FIG. 38. The latched data 456 is taken in the CPU 301 by the read signal 451 at a time indicated by data 458 in FIG. 39. There is no problem in the case shown in FIG. 38 in which the data is taken in the CPU 301 at a time other than a transition of the data 456.

However, the above-described conventional technique has the following disadvantages.

In the case of the signal whose one bit has a significance, like the signals 401 and 402 shown in FIG. 33 and like the signals 410 and 411 shown in FIG. 34, there is no problem. However, in the case of a significant signal consisting of a plurality of bits, since transition does not occur on the individual bits simultaneously, erroneous transmission may occur.

That is, in a case where the transmission means 409 latches data at the transition of the data 454, as shown in FIG. 39, the transmit data subsequent to a reference number 459 is not guaranteed. Also, in a case where the CPU 301 reads in data at the transition of the data 456, as shown in FIG. 40, data subsequent to 460 is not guaranteed.

In order to avoid this disadvantage, a handshake may be conducted in terms of software or hardware between the CPU 301 and the transmission means 409 or between the CPU 301 and the reception means 414. However, this requires complicated additional circuits and hence increases the production cost of the system.

(3) Parallel connection between a communication device (hereinafter referred to as a master) of the main control portion and the communication device (hereinafter referred to as a slave) of each of the group of units is easily affected by noise or the like. In the case of a series connection, the unit to be controlled independently may affect or be affected by other units.

When the operation of a system is to be controlled utilizing the serial communication for the exchange of information between the central processing unit for executing the main control of the system and the individual units which scatter in the system, the system is conventionally structured in the manner shown in FIG. 45.

In FIG. 45, a master 550 is a main communication device in the central processing unit which controls serial communication. Slaves 551 to 554 are sub-communication devices in the individual units scattered in the system which conduct serial communication and executes information exchange.

In this serial communication, the master and slaves make 1-to-N correspondence. Therefore, exchange of serial data signal is conducted between the main communication device and the individual sub-communication devices which are parallel-connected to the main communication device independently.

Therefore, in the above-described conventional system, the communication lines for the serial data signal are extended over a long distance because of parallel connection, causing malfunction to occur due to the noise generated within the system. Furthermore, its drive ability of the master communication device must be enhanced by providing a drive means in the master communication device. This may increase the production cost.

Furthermore, in the case of a unit that can be detachably mounted by a user, the serial data signal lines may

	Document ID	U	Title	Current OR
1	US 20040054879 A1	☐	Method and apparatus for parallel table lookup using SIMD instructions	712/221
2	US 20040054878 A1	☒	Method and apparatus for rearranging data between multiple registers	712/221
3	US 20040054877 A1	☒	Method and apparatus for shuffling data	712/221
4	US 20040018018 A1	☒	Optical code-division multiple access transmission system and method	398/77
5	US 20040011948 A1	☒	High accuracy miniature grating encoder readhead using fiber optic receiver channels	250/231.13
6	US 20030210674 A1	☒	Method for scheduling packet data transmission	370/338
7	US 20030103476 A1	☒	Method for measuring confusion rate of a common packet channel in a CDMA communication system	370/329
8	US 20020141589 A1	☒	Cryptographic key processing and storage	380/277
9	US 20020116602 A1	☒	Partial bitwise permutations	712/223
10	US 20020091916 A1	☒	Embedded-DRAM-DSP architecture	712/228
11	US 20020087845 A1	☒	Embedded-DRAM-DSP architecture	712/228
12	US 20020040429 A1	☒	Embedded-DRAM-DSP architecture	712/228
13	US 20020013926 A1	☒	Apparatus and method for encoding and decoding TFCI in a mobile communication system	714/781
14	US 20010053140 A1	☒	Apparatus and method for assigning a common packet channel in a CDMA communication system	370/335
15	US 20010046220 A1	☒	Apparatus and method for assigning a common packet channel in a CDMA communication system	370/335
16	US 20010026543 A1	☒	Apparatus and method for assigning a common packet channel in a CDMA communication system	370/335
17	US 20010012360 A1	☒	Method of executing a cryptographic protocol between two electronic entities	380/29

directly receive external noise from the connector of the detachably mounted unit, which leads to breakage of the main control unit. This increases maintenance cost.

Furthermore, in a case where an abnormality occurs in the system, the sub-communication device in a certain unit may be forcibly reset in order to turn off all the actuators or the like connected to that sub-communication device. In another unit, serial communication may be continued for anomaly processing. These necessitate independent parallel connection between the main communication device and the individual sub-communication devices. For example, in a laser beam printer, if paper jam occurs during the paper feeding operation, high-voltage output must be stopped instantaneously in order to protect a light-sensitive drum or the like. However, interruption of the paper feeding logic and restarting of the paper feed after jam has been removed may cause a jam again.

SUMMARY OF THE INVENTION

In view of the overcoming of the disadvantage of the conventional technique described in Item (1), an object of the present invention is to provide a unit control oriented communication device which is free from malfunctioning due to transmission of erroneous data caused by noises or disturbances.

Another object of the present invention is to provide a unit control oriented communication device which is capable of preventing collision of data which would occur in the bidirectional transfer of data, of eliminating erroneous transmission of data, and of high-speed transmission.

Another object of the present invention is to provide a unit control oriented communication device which is capable of overcoming problems, such as the erroneous transmission of data, caused by collision of light or disturbances, which would occur when data is transmitted in two directions during optical communication, and of preventing the generation of data from the disturbance data.

Another object of the present invention is to provide a unit control oriented communication device which is free from communication run-away caused by the generation of communication errors.

Another object of the present invention is to provide a unit control oriented communication device which is capable of recognizing existence and non-existence of units.

Another object of the present invention is to provide a unit control oriented communication device which is capable of discriminating a communication error and non-existence of the unit.

Another object of the present invention is to provide a unit control oriented communication device which can simply be adjusted or checked for assembly and which is hence effective.

Another object of the present invention is to provide a unit control oriented communication device which does not fail to enter the self-diagnosis mode due to a communication error which occurs accidently.

In order to achieve the aforementioned objects, the present invention provides a unit control oriented communication device which is for use in a system, including a group of a plurality of units each of which is the physical or functional unit of scattered output and input signals and a main control portion for controlling the group of units, for serially transmitting information between the main control portion and the group of units. The unit control oriented communication device comprises at least one error detection function selected from first, second and third detection functions. The first detection function includes a modulation/demodulation means for conducting modulation or demodulation on the basis of a predetermined rule, and a first error detection means for detecting an communication error in accordance with the predetermined rule. The second error detection function includes a transmit data creation/analysis means for creating serial data which is to be transmitted in a state in which it contains positive data and negative data of the same bit in one frame which is the unit of communication and for analyzing the serial data when it is received, and a second error detection means for detecting a communication error on the basis of the comparison between the positive and negative data. The third error detection function includes a space bit addition/separation means for creating the serial data which is to be transmitted in a state in which a predetermined space bit is added in the one frame and for separating the space bit when the serial data is received, and a third error detection means for detecting a communication error on the basis of the timing in which the space bit and effective bits appear.

The present invention further provides a unit control oriented communication device which comprises a first reception inhibit means for inhibiting data reception during data transmission, and a second reception inhibit means for inhibiting the starting of reception of another data in a predetermined period of time after receive data is received.

The present invention further provides a unit control oriented communication device which comprises a counting means for conducting counting when there is no reply to the transmitted data, and an error discrimination means for discriminating a communication error when the count of the counting means reaches a predetermined value.

The present invention further provides a unit control oriented communication device which comprises a number addition means for adding to the transmit/-receive data a peculiar number which specifies the unit, and a discrimination means for discriminating a communication error and non-existence of the unit in accordance with the presence or absence of a reply from the individual communication device in the group of units which is based on the peculiar numbers.

The present invention further provides a unit control oriented communication device which comprises a first transmission inhibit means for inhibiting data transmission during data reception, and a second transmission inhibit means for inhibiting transmission of data when an error is detected in the receive data.

The present invention further provides a unit control oriented communication device which comprises a register means for registering peculiar numbers which specify switch over of the individual units in the unit group to the test mode, and a self-diagnosis means for attaining the test mode and conducting self-diagnosis in a case where the peculiar number in receive data is the peculiar number registered by the register means.

The present invention further provides a unit control oriented communication device which comprises a reply means for returning a reply only from the serial communication device in the unit which is registered by a peculiar number designated in received data, a peculiar number determination means for determining

	Document ID	U	Title	Current OR
18	US 6721349 B1	☒	Method and apparatus for reducing peak-to-average ratio in a CDMA communication system	375/130
19	US 6715066 B1	☒	System and method for arranging bits of a data word in accordance with a mask	712/300
20	US 6700991 B1	☒	Hidden digital watermarks in images	382/100
21	US 6674739 B1	☒	Device and method for assigning spreading code for reverse common channel message in CDMA communication system	370/342
22	US 6674712 B1	☒	Device and method for generating quaternary complex quasi-orthogonal code and spreading transmission signal using quasi-orthogonal code in CDMA communication system	370/208
23	US 6629239 B1	☒	System and method for unpacking and merging bits of a data world in accordance with bits of a mask word	712/300
24	US 6584089 B1	☒	Method for scheduling packet data transmission	370/338
25	US 6564162 B1	☒	Method and apparatus for improving electrical verification throughput via comparison of operating-point differentiated test results	702/120
26	US 6519239 B1	☒	Method and apparatus for providing dispatch service in a CDMA communication system	370/335
27	US 6188767 B1	☒	Method of providing group call services in a CDMA communications system	380/271
28	US 6094426 A	☒	Method for scheduling packet data transmission	370/331
29	US 6091717 A	☒	Method for scheduling packet data transmission	370/329
30	US 5995715 A	☒	Method and apparatus for reducing strip effect caused by printers	358/1.9
31	US 5872965 A	☒	System and method for performing multiway branches using a visual instruction set	712/236
32	US 5771288 A	☒	Multiple access coding for radio communications	380/270
33	US 5742678 A	☒	Multiple access coding for radio communications	380/270
34	US 5717760 A	☒	Message protection system and method	380/28
35	US 5652900 A	☒	Data processor having 2n bits width data bus for context switching function	718/100
36	US 5631089 A	☒	Preparation of glass/plastic laminates having improved optical quality	428/437
37	US 5560036 A	☒	Data processing having incircuit emulation function	712/227
38	US 5550809 A	☒	Multiple access coding using bent sequences for mobile radio communications	370/342
39	US 5502827 A	☒	Pipelined data processor for floating point and integer operation with exception handling	712/244
40	US 5481734 A	☒	Data processor having 2n bits width data bus for context switching function	712/225

whether or not the peculiar number designated in the receive data is the register number of the main control portion, and a self-diagnosis means for suspending the serial communication and for attaining the test mode independently in a case where it is determined by the peculiar number determination means that the peculiar number in the received data is the register number of the main control portion.

In view of the overcoming of the disadvantage of the conventional technique described in Item (2), an object of the present invention is to provide a unit control oriented communication device which is capable of exchanging reliable data using a simplified circuit configuration for the control of the control subjects.

In order to achieve the above-described object, the present invention provides a unit control oriented communication device which comprises a microprocessor, a transmission means for transmitting transmit data to control subjects which are controlled by the microprocessor, and a transmission data register for storing the transmit data to be transferred from the microprocessor to the transmission means. The transmission means has a read request signal generation means for outputting a read request signal when the transmission means receives data from the transmission data register. The unit control oriented communication device further includes a read signal generation means for generating a read signal for the transmission data register from the read request signal and a signal dependent on the machine cycle of the microprocessor.

The reception means has a write request signal generation means for outputting a write request signal when the reception means writes the receive data in the reception data register. The unit control oriented communication device further comprises a write signal generation means for generating a write signal for the reception data register from the write request signal and a signal dependent on the machine cycle of the microprocessor.

In view of the overcoming of the disadvantage of the conventional technique described in Item (3), an object of the present invention is to provide a unit control oriented communication device which is capable of achieving a series connection in a physical fashion, and a parallel connection in an electrical fashion, between the master communication device and the slave communication devices.

In order to achieve the above-described object, the present invention provides a unit control oriented communication device designed for exchanging information within a system to achieve control of the operation of the system. The unit control oriented communication device includes a means for receiving a communication signal, and a means for transferring the received communication signal to another communication device, transfer of the received communication signal being possible even when the communication device is set to a reset state.

Other objects, features and advantages of the invention will be apparent from the following description taken in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1, comprised of FIGS. 1A and 1B, is a block diagram of a communication means for an embodiment of a unit control oriented communication device according to the present invention;

FIG. 2 shows modulating and demodulating circuits shown in FIG. 1 in detail;

FIGS. 3, comprised of FIGS. 3A and 3B, and 4, comprised of FIGS. 4A and 4B, are timing charts of the circuit shown in FIG. 2;

FIG. 5, comprised of FIGS. 5A and 5B, shows a comparison/selection circuit of FIG. 1 in detail;

FIG. 6 shows the comparison conditions of the comparison/selection circuit;

FIGS. 7, comprised of FIGS. 7A and 7B, and 8, comprised of FIGS 8A and 8B, are timing charts of the circuit shown in FIG. 5;

FIGS. 9, comprised of FIGS. 9A and 9B, and 10, comprised of FIGS. 10A and 10B, show modifications of the embodiment shown in FIG. 1;

FIG. 11 shows a system to which the communication means of FIG. 1 is applied;

FIG. 12 shows frequency division control conducted when the communication means of FIG. 1 is used in a master device;

FIG. 13 shows frequency division control conducted when the communication means of FIG. 1 is used in a slave device;

FIG. 14 shows a circuit for returning an error when reception error occurs;

FIG. 15, comprised of FIGS. 15A and 15B, is a timing chart of the circuit shown in FIG. 14;

FIGS. 16 and 17 shows examples of the circuit for detecting communication errors;

FIG. 18 shows a circuit used in the test mode in the master device;

FIG. 19 is a flowchart of the control of a CPU 105;

FIG. 20, comprised of FIGS. 20A and 20B, shows a circuit used in the test mode in the slave device;

FIG. 21 is a block diagram showing a system configuration of the embodiment of the present invention;

FIG. 22 is a circuit diagram of the vicinity of a transmission register 304 shown in FIG. 21;

FIG. 23 is a timing chart of the operation of outputting data to the transmission register 304;

FIG. 24 is a timing chart of the operation of inputting data in and outputting data from the transmission register 304;

FIG. 25 is a block diagram showing a system configuration of another embodiment of the present invention;

FIG. 26 is a circuit diagram of the vicinity of a reception register 321 shown in FIG. 25;

FIG. 27 is a timing chart of the operation of reading out data from the reception register 321;

FIG. 28 is a timing chart of the operation of inputting data in and outputting data from the reception register;

FIGS. 29 and 30 are timing charts of the operation in still another embodiment of the present invention;

FIGS. 31 to 34 are block diagrams showing the configuration of a conventional technique;

FIGS. 35 and 36 are circuit diagrams of the vicinity of a transmission register 408 and that of a reception register 415 which are respectively shown in FIGS. 33 and 34;

FIGS. 37 to 40 are timing charts of the operations in the configurations shown in FIGS. 33 and 34;

FIG. 41 is a block diagram of the unit employed in the embodiment of the present invention;

FIG. 42 is a block diagram of a slave communication device of the embodiment;

FIG. 43 is a block diagram showing the connection form in the embodiment;

	Document ID	U	Title	Current OR
41	US 5440757 A	☒	Data processor having multistage store buffer for processing exceptions	712/228
42	US 5386522 A	☒	Dynamic physical address aliasing during program debugging	717/124
43	US 5353352 A	☒	Multiple access coding for radio communications	380/37
44	US 5214701 A	☒	Method of processing data by compression and permutation for microcircuit cards	380/29
45	US 5193115 A	☒	Pseudo-random choice cipher and method	380/46
46	US 5168521 A	☒	Method of executing an irregular permutation of data protected by encryption	380/29
47	US 5113444 A	☒	Random choice cipher system and method	380/47
48	US 5023157 A	☒	Method for the illumination of a color television mask tube screen, and device for implementation thereof	430/24
49	US 4656580 A	☒	Logic simulation machine	703/19
50	US 4435838 A	☒	Method and apparatus for tomographical imaging	382/312
51	US 4355235 A	☒	Devices for measuring parameters which can modify the charge of an electret	250/376
52	US 4306286 A	☒	Logic simulation machine	703/15
53	US 3936806 A	☒	Solid state associative processor organization	712/10
54	US 3705357 A	☒	MORPHIC EXCLUSIVE-OR CIRCUITS	326/52
55	US 3553466 A	☒	PLURALITY OF LONGITUDINALLY SCANNED FLUORESCENT LIGHT-CONDUCTIVE FIBERS DIFFERENTIALLY MASKED FOR BEAM POSITION DETECTION	250/227.11

FIG. 44 is a block diagram showing another embodiment; and

FIG. 45 is a block diagram showing the connection form in the conventional communication device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be described below with reference to the accompanying drawings.

SERIAL COMMUNICATION MEANS

FIG. 1 is a block diagram of a serial communication means of this embodiment.

The serial communication means includes a ½ frequency dividing circuit 1 for decreasing a system driving clock by a factor of two, a multiple frequency dividing circuit 2, a timing generating circuit 3 for outputting a desired timing signal on the basis of a clock input from the multiple frequency dividing circuit 2, a synchronizing circuit 4 for synchronizing received serial data, a frequency-division control circuit 5 for reactivating the multiple frequency dividing circuit 2 in a timing obtained by the synchronizing circuit, a demodulating/-converting circuit 6 for converting received modulated data into binary data, and an error detecting circuit 7 for detecting an error caused by conversion or noises during the demodulation of the decoding/converting circuit 6.

The serial communication means further includes an ID data input circuit 8 for inputting an ID number representing the attribute of the serial communication means, a data input circuit 9 for inputting transmit data of the serial communication means, a data output circuit 10 for outputting receive data of this serial communication means, a positive logic ID data output circuit 11 and a negative logic ID data output circuit 12 for separating the ID data obtained by the ID data input circuit 8 into positive logic data and negative logic data to obtain transmit data, a positive logic data output circuit 13 and a negative logic data output circuit 14 for separating the transmit data obtained by the data input circuit 9 into positive logic data and negative logic data to obtain transmit data, and a data encoder circuit 15 for creating binary data of the transmit data to be transmitted from this serial communication means and for outputting the same to an 8-bit shift register 16 in a transmission timing.

The serial communication means further includes the 8-bit shift register 16 for shift latching the binary data of the receive data which is obtained by the synchronizing circuit 4 and the decoding/converting circuit 6 and for shift outputting the transmit data output from the data encoding circuit 15, shift data latch circuits 17, 18 and 19 for latching the binary data shift input by the 8-bit shift register 16 in a timing generated by the timing generating circuit 3, three shift data latching circuits being provided in this embodiment for conducting latching on one frame three times, and a comparing-/selecting circuit 20 for comparing data latched by the shift data latching circuits 17, 18 and 19 under a predetermined condition and for selecting necessary data to determine the truth or falsity of receive data.

A modulating/converting circuit 21 modulates the binary transmit data output from the 8 bit shift register 16 under a predetermined condition, i.e., for conducting an operation reverse to that of the demodulating/converting circuit 6, to obtain serial transmit data. An AND gate 22 controls a latch signal for inputting data in the data output circuit 10 on the basis of the result of the comparison made by the comparing/selecting circuit 20.

To simplify the description, the circuit configuration of this embodiment is in 8-bit unit. However, it may be in 16- or 32-bit unit.

The operation of the serial communication means shown in FIG. 1 will be described below. A system clock of this system enters the ½ frequency dividing circuit 1 which arranges the clock such that it has 50% duty factor. The output clock is used as the operation clock for the synchronizing circuit 4 and that of the frequency-division control circuit 5. The output clock is also input to the multiple frequency dividing circuit 2 which outputs the clocks obtained by division of "2^{11}" to the timing generating circuit 3 and thereby make it generate a desired timing which will be described later. The internal configuration of the circuits 1, 2, 3, 4 and 5 is a known one, and a detailed description thereof is therefore omitted. Therefore, the configuration thereof is not limited to the above-described one but various modifications are possible if they attain the objectives described in this specification.

Input/output of data into and from this serial communication means will be described below. In FIG. 1, the serial data input input to the synchronizing circuit 4 is the receive data input. This receive data is output from the data output circuit 10 as the receive data output. The ID data input and the transmit data input, which are input to the input circuits 8 and 9, are output from the modulating/converting circuit 21 as the serial data output. The ID data input is used to determine the truth of the receive data input, and the details thereof will be described later.

FIG. 2 shows the modulating and demodulating circuits shown in FIG. 1 in detail.

First, the operation of the modulating/converting circuit 21 will be described. In FIG. 2, data (j) output from a shift out terminal of the 8-bit shift register 1 is input to an EXOR 212 in the modulating/converting circuit 21. A clock ϕ_{32} obtained by decreasing the output of the ½ frequency dividing circuit 1 by a factor of 32 by means of the multiple frequency dividing circuit 2 is inverted by an inverting gate 211 to adjust the phase thereof, and the inverted signal (g) is input to the other input of the EXOR circuit 212 in the modulating/converting circuit 21. The EXOR circuit 212 outputs a serial data signal (k) to be transmitted. The modulation attained in the above-described circuit will be described in detail.

The shift out data (j) is sequentially output by the clock of ϕ_{32}. EXOR operation is conducted on the shift out data (j) and the inverted signal of the clock ϕ_{32}. That is, if "1" is shifted out, "10" is output from the EXOR circuit 212. Also, if "0" is shifted out, "01" is output from the EXOR circuit 212. Thus, if the transmit data is "1011000100 . . . ", "10 01 10 10 01 01 01 10 01 01 . . . " is output from the modulating/converting circuit 21 under the conditions of this modulation method. Hence, this transmit data will be demodulated at the reception side by inverting this transmit data and then by latching data alternately starting from the second one (by latching odd numbers). The same demodulation results can be obtained by latching the data alternately starting from the first one (by latching even numbers) and then conducting demodulation. Concrete

	L #	Hits	Search Text	DBs
1	L1	351267	(reorder$3 order$3 rearrang$3 arrang$3) near10 (bit byte element item)	USPAT; US-PGPUB
2	L5	2000	(swap$4 centrifug$3 shift$3 exchang$3) near10 (element item bit byte) near20 mask$3	USPAT; US-PGPUB
3	L6	209	(reorder$3 order$3 rearrang$3 arrang$3).ab,ti. and 1 and 5	USPAT; US-PGPUB
4	L7	150	1 near99 5	USPAT; US-PGPUB
5	L8	164	6 not 7	USPAT; US-PGPUB

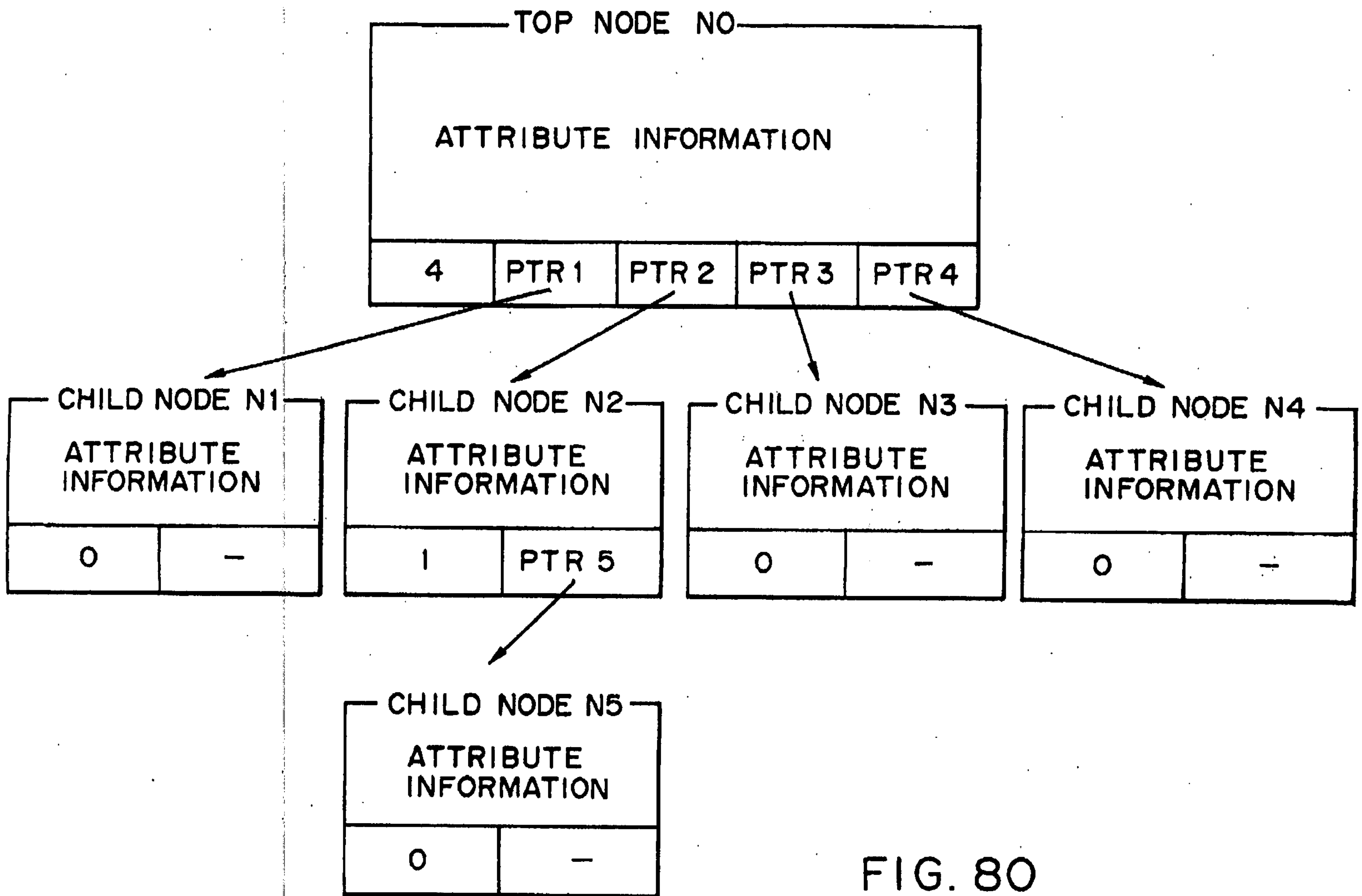
TOP NODE NO
ATTRIBUTE INFORMATION
4
PTR 1
PTR 2
PTR 3
PTR 4
CHILD NODE N1
ATTRIBUTE INFORMATION
0
–
CHILD NODE N2
ATTRIBUTE INFORMATION
1
PTR 5
CHILD NODE N3
ATTRIBUTE INFORMATION
0
–
CHILD NODE N4
ATTRIBUTE INFORMATION
0
–
CHILD NODE N5
ATTRIBUTE INFORMATION
0
–

FIG. 80

	L #	Hits	Search Text	DBs
1	L1	351267	(reorder$3 order$3 rearrang$3 arrang$3) near10 (bit byte element item)	USPAT; US-PGPUB
2	L5	2000	(swap$4 centrifug$3 shift$3 exchang$3) near10 (element item bit byte) near20 mask$3	USPAT; US-PGPUB
3	L6	209	(reorder$3 order$3 rearrang$3 arrang$3).ab,ti. and 1 and 5	USPAT; US-PGPUB
4	L7	150	1 near99 5	USPAT; US-PGPUB
5	L8	164	6 not 7	USPAT; US-PGPUB
6	L9	170489	(reorder$3 order$3 rearrang$3 arrang$3) near10 (bit byte element item)	EPO; JPO; DERWENT; IBM_TDB
7	L10	442	(swap$4 centrifug$3 shift$3 exchang$3) near10 (element item bit byte) near20 mask$3	EPO; JPO; DERWENT; IBM_TDB
8	L11	55	9 and 10	EPO; JPO; DERWENT; IBM_TDB

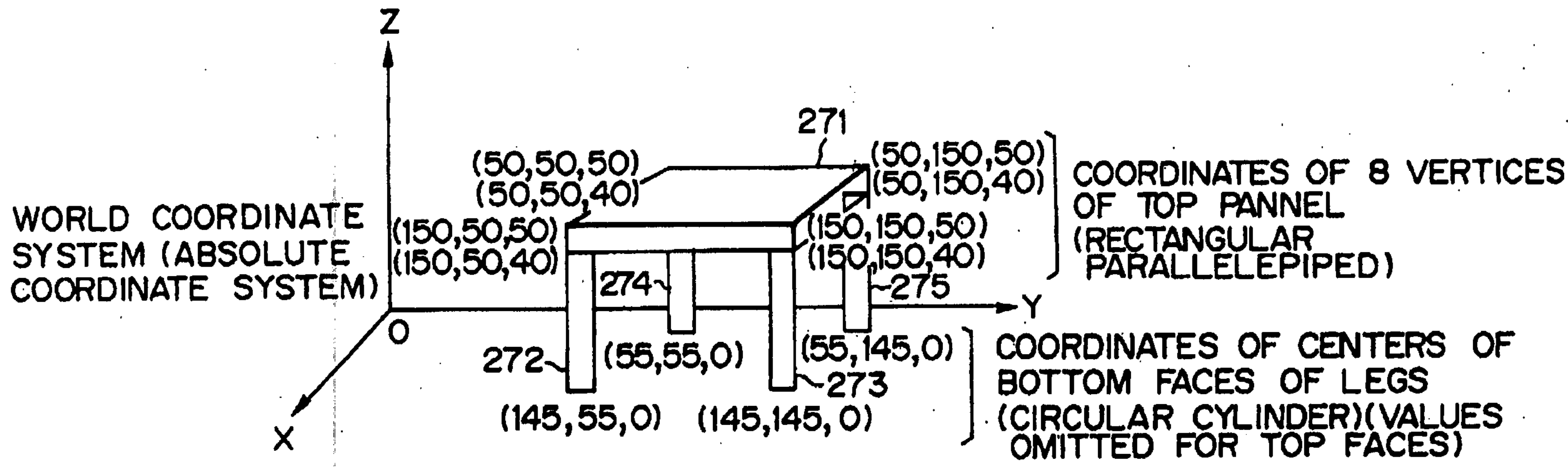
WORLD COORDINATE SYSTEM (ABSOLUTE COORDINATE SYSTEM)
Z
Y
X
O
271
272
273
274
275
(50,50,50)
(50,50,40)
(150,50,50)
(150,50,40)
(50,150,50)
(50,150,40)
(150,150,50)
(150,150,40)
COORDINATES OF 8 VERTICES OF TOP PANNEL (RECTANGULAR PARALLELEPIPED)
(55,55,0)
(145,55,0)
(55,145,0)
(145,145,0)
COORDINATES OF CENTERS OF BOTTOM FACES OF LEGS (CIRCULAR CYLINDER)(VALUES OMITTED FOR TOP FACES)

FIG. 81